What is claimed is:

Claim 1

A method for programming bit data to a nonvolatile semiconductor memory device, said nonvolatile semiconductor memory device comprising,

an n type well formed in a semiconductor substrate,

a source and a drain of p+ regions formed in the surface of said n type well with a predetermined interval,

a channel region formed between said source and said drain,

a charge accumulation layer of a floating gate, a nano-crystal layer, a nonconductive charge trap layer such as a silicon nitride layer, and so on, formed above said channel region via a tunnel insulating layer, and

a gate electrode formed above said charge accumulation layer via an insulating layer,

said method comprising:

applying Vg, Vsub, Vs and Vd to the gate electrode, the n type well, the source and the drain respectively during programming, the Vg, the Vsub, the Vs and the Vd being in a relationship of "Vg>Vsub>Vs>Vd" and "Vg-Vd" being not less than an electrical potential difference necessary to generate a band to band tunneling current at said channel

region,

thereby generating hot electrons near the drain by band to band tunneling, and

injecting said hot electrons into said charge accumulation layer to program the bit data.

Claim 2

A method for programming bit data to a nonvolatile semiconductor memory device, said nonvolatile semiconductor memory device comprising,

a p type well formed in a semiconductor substrate,

a source and a drain of n+ regions formed in the surface of said p type well with a predetermined interval,

a channel region formed between said source and said drain,

a charge accumulation layer of a floating gate, a nano-crystal layer, a nonconductive charge trap layer such as a silicon nitride layer, and so on, formed above said channel region via tunnel insulating layer, and

a gate electrode formed above said charge accumulation layer via an insulating layer,

said method comprising,

applying Vg, Vsub, Vs, and Vd to the gate electrode, the p type well the source and the drain respectively during

programming, the Vg, the Vsub, the Vs, and the Vd being in a relationship of "Vg<Vsub<Vs<Vd" and "Vd-Vg" being not less than an electrical potential difference necessary to generate a band to band tunneling current at said channel region,

thereby generating hot holes near the drain by band to band tunneling, and

injecting said hot holes into said charge accumulation layer to program the bit data.

Claim 3

A method for programming to a nonvolatile semiconductor memory device according to claim 1 or claim 2, two of the voltages from said Vg, Vsub, Vs and Vd are supplied from an external power supply.

Claim 4

A method for programming to a nonvolatile semiconductor memory device according to claim 1 or claim 2, at least the Vd among said Vg, Vsub, Vs and Vd is supplied from an external power supply.

Claim 5

A method for programming to a nonvolatile

semiconductor memory device according to claim 1 or claim 2, the Vs and the Vd among said Vg, Vsub, Vs and Vd are supplied from an external power supply.

Claim 6

A method for programming to a nonvolatile semiconductor memory device according to claim 5, said Vs is a power supply voltage and the Vd is a ground voltage.

Claim 7

A nonvolatile semiconductor memory device having memory cells programmed by the method of claim 1 or claim 2, and arrayed by connecting in a NOR type or in a NAND type.